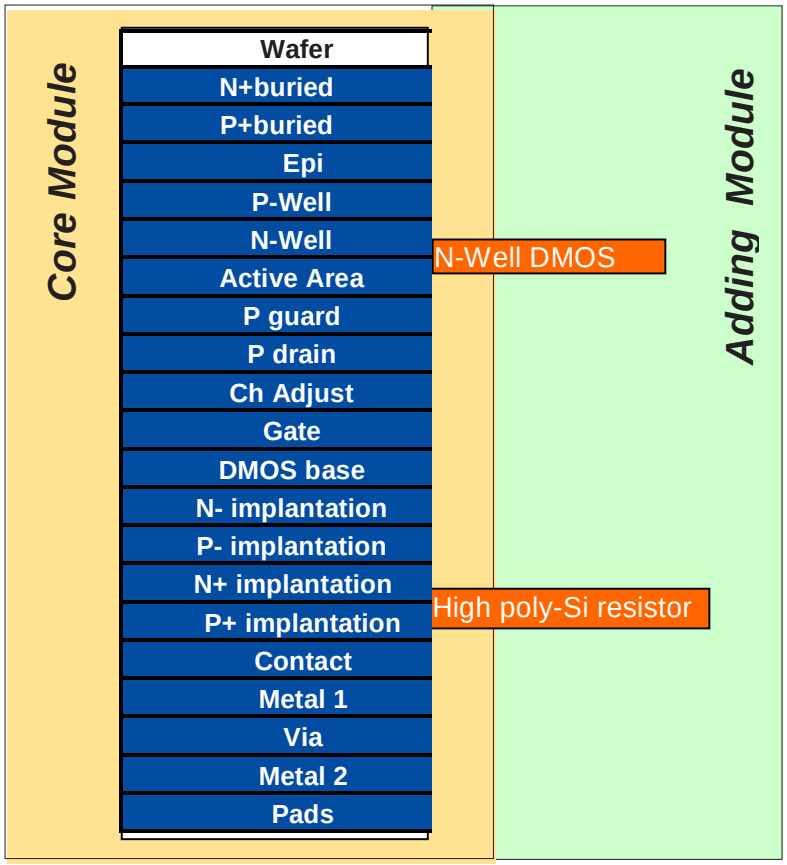
DMS LAB Limited

20-30V BiCDMOS process specification

Description

- 20-30V 0.8um BiCDMOS process is DMS Lab Limited BCD smart power technologies. Main target applications are analog switch ICs, DC-DC converters, driver ICs for capacitive, inductive and resistive loads for applications using 20-30V supply. The typical breakdown voltage of the DMOS devices more than 20V, 30V accordingly.
- The modular process combines DMOS and HV CMOS for different supply application with core bipolar, logic CMOS processing steps to provide a wide variety of MOS and bipolar devices with different voltage levels on the same die.
- The 19 layers core process module is available for 20V breakdown voltage of the DMOS. This process module provides locos insulation, single level poly, and two metal levels.
- With this core module an optimized self-aligned poly-gate n-channel lateral DMOS transistor, HV CMOS, logic CMOS and some bipolar transistors can be made,
- Other process modules can be added to integrate 30V NDMOS transistors (1 layer), high value poly-Si resistors and poly1-poly2 capacitors (1 layer).



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> Key Features

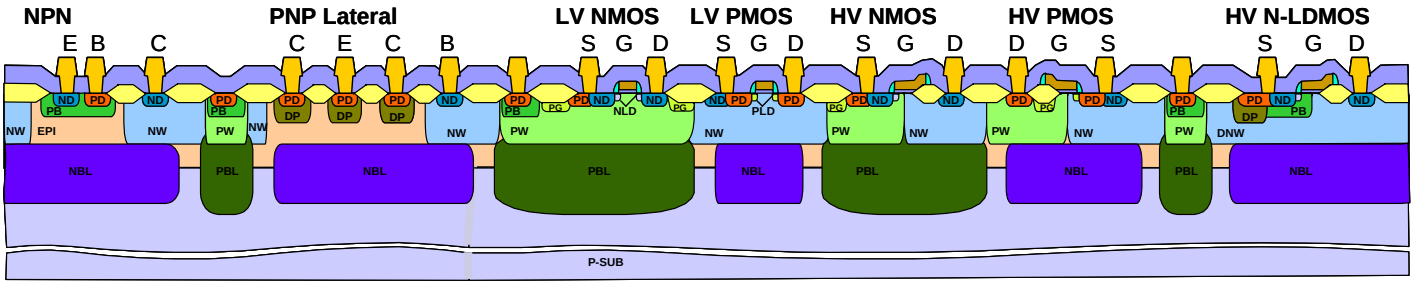
The lateral DMOS transistor with low Rdson and small area is the main HV component of the BiCDMOS 20-30V technology. The device structure and process parameters are optimized to obtain a drain breakdown voltage of >25V and >35V and maximum drain saturation current with a low on-resistance.

0.8um one poly, double metal, double Well BCD process.

A high number of different devices are available:

- 20V or 30V (optional) n-channel LDMOS transistor;
- 30V n-channel MOS transistor;
- 30V p-channel MOS transistor;
- Logical 5V CMOS transistors;
- 5V and 20V NPN transistors;
- 5V and 20V PNP transistors;
- Zener diodes and Schottky diodes;
- Gate oxide capacitors;
- Low resistivity poly-Si resistors;
- Resistors in active layers.
    - Optional poly for high value resistor;
    - Optional poly-1 – poly2 capacitors;

> Schematic cross section



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> Basic design rules

Layer	Min width (um)	Min spacing (um)
Active Area (CMOS)	2.0	1.5
CMOS Gate	0.8	0.8
DMOS Gate	2.0	1.5
Contact	0.8	0.8
Metal-1	1.2	1.0
VIA	0.8	1.2
Metal-2	1.5	1.3

〉 Device Parameters of main elements for 20-30V process

ELEMENT	PARAMETER	SPEC		MEASUREMENT CONDITIONS
	UNIT	MIN	MAX	
HV NDMOS L=2 um, W=20 um	VTH, V	0.7	1.4	Id=0.1uA
	IDS, mA	8.0	-	Ug=Ud=5 V
	BVDS, V	25 (35)	-	Id=10uA
	Rsp, mOhm*mm2	-	45 (40)	Ug=10 V
	IDS, uA	-	50	Ug=Ub=Us=0 V, Ud =10 V
HV NMOS L=7.0 um, W=56 um	VTH, V	0.5	0.9	Id=0.1uA
	IDS, mA	0.5	-	Ug=Ud=10 V
	BVDS, V	35	-	Id=10uA
HV PMOS L=6.0 um, W=50 um	VTH, V	0.7	1.1	Id=0.1uA
	IDS, mA	0.35	-	Ug=Ud=10 V
	BVDS, V	35	-	Id=10uA
LV NMOS L=0.8 um, W=50 um	VTH, V	0.5	0.9	Id=0.1uA
	IDS, mA	15	25	Ug=Ud=5 V
	BVDS, V	8.0	-	Id=10uA
LV PMOS L=0.8 um, W=50 um	VTH, V	0.7	1.1	Id=0.1uA
	IDS, mA	7.0	12	Ug=Ud=5 V
	BVDS, V	10	-	Id=10uA
HV NPN Se=10x10 um2	BETA	30	100	Ib=10uA, Uc=1 V
	BVCE0, V	35	-	Ic=10uA, floating base
LV NPN Se=10x10 um2	BETA	30	100	Ib=10uA, Uc=1 V
	BVCE0, V	9	-	Ic=10uA, floating base
HV Lateral PNP Wb=5um	BETA	15	-	Ib=-10uA, Uc=-1 V
	BVCE0, V	25	-	Ic=-10uA, floating base
LV Lateral PNP Wb=4um	BETA	15	-	Ib=-10uA, Uc=-1 V
	BVCE0, V	9	-	Ic=-10uA, floating base
Schottky Diode	BV, V	30	-	Id=10uA
Zener Diode	BV, V	5.5	6.5	Id=10uA
Base Resistor	RS, Ohm/sq	450	550	Ir=10uA
PolySi- gate oxide – Well capacitor	Ccs, pF/um2	1,7E-3	2.1E-3	F=1MHz, Vmea=5V
Note: ( ) – value for option (adding module)				